



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Neil McLoughlin  
Appl. No.: 09/737,596  
Filed: December 18, 2000  
Title: NICKEL BARRIER END TERMINATION AND METHOD  
Art Unit: 2832  
Examiner: K. Easthom  
Docket No.: 112690-895

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

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Reconsider.  
Hawkins  
9/16/03

**REQUEST FOR RECONSIDERATION**

Dear Sir:

In response to the non-final Office Action of April 2, 2003, the Applicant respectfully requests reconsideration of the rejections in light of the following remarks.

**REMARKS**

Claims 36 and 38-51 are pending in the present application. All of these claims stand rejected. The Applicant requests reconsideration of the rejections based on the following comments.

Claims 36 and 38-51 were rejected under 35 U.S.C. §103(a) as being unpatentable over Chan or Ravindranathan in view of Ueda (Japanese Patent No. 3-225802) and further in view of the disclosed prior art on pages 1-2 of the present application. The Applicant respectfully traverses this rejection for the following reasons.

In rejecting the claims, the Office Actions asserts that the features of the claims are disclosed except for the interior body not being contacted. Ueda is asserted as disclosing termination of a thermistor, in particular, without contacting an interior body. The rejection, however, is devoid of any provision of motivation to combine the cited references and, furthermore, does not teach or suggest all of the elements of claim 36, in particular.

Specifically with respect to claim 36, although Ueda illustrates coating an electrode material paste for on a chip type thermistor, Ueda could hardly be characterized as disclosing terminations on a thermistor without contacting interior body. To the contrary, the process illustrated in Figure 4 of Ueda illustrates coating the thermistor element for a distance up to a notch 2. Furthermore, as illustrated in Figures 2 and 3 of Ueda, a significant portion of an interior region of the thermistor is encroached upon by the electrode part 3.

Moreover, the Office Action has not provided proper motivation to combine the cited references. Specifically, with respect to the combination of Chan, Ueda and the disclosed art, the Applicant submits that one of ordinary skill in the art would not modify Chan, which teaches

applying a nickel barrier using sputtering, with the putative dipping process of Ueda. Such a combination would change the principle of operation of Chan (i.e., sputtering deposition of the nickel barrier), thus evincing a lack of motivation to combine to one of ordinary skill in the art.

With respect to the combination of Ravindranathan in view of Ueda and the disclosed prior art in the present application, motivation to combine these references is lacking and all of the elements are not taught. Specifically, Ravindranathan teaches first treating a body 22 with a phosphoric acid solution to provide a zinc phosphate layer 34 (see, col. 3, ll. 1-19). In other words, the body surface is treated, whereas claim 36 features a semiconductor body having a body surface that is untreated. Moreover, the terminal regions 32 of the body 22 in Ravindranathan are electrically connected to electrically conductive metals (preferably silver, silver-platinum, or silver-palladium) end terminations 30. Only after the zinc phosphate layer 34 has been applied by spraying or submersion, is a metal plating of layers 36 comprised of nickel or tin-lead applied using a conventional barrel plating process (see, col. 3, ll. 20-30). Thus, even if the teachings of Ueda were combined with Ravindranathan, all of the elements of claim 36 are not met because the body surface of Ravindranathan is treated prior to forming nickel end terminations, whether by barrel plating process or the putative dipping process of Ueda. Further, one of ordinary skill in the art would not be motivated to combine these references to arrive at the claimed elements since claim 36 requires nickel barrier caps formed directly on untreated terminal regions, whereas Ravindranathan clearly teaches application end terminations 30 of silver, silver-palladium or silver-platinum prior to application of nickel. To discard these end terminations 30 would change the principle of operation of Ravindranathan, thus rendering the combination without a proper motivation or suggestion to combine.

Accordingly, in light of the foregoing comments the Applicant respectfully submits that claim 36 is not obvious in view of the prior art of record and requests that the rejection of this claim be withdrawn.

With respect to claim 38, this claim is believed to be allowable at least by virtue of its dependency on independent claim 36.

With respect to independent claim 39, although Chan may incorporate Utsumi by incorporation, this reference is nonetheless described as related art and does not teach or suggest the features of claim 24 including a semiconductor body having an untreated body surface. Furthermore, no motivation exists to combine the teachings of Ueda with Chan because, as discussed previously, Chan explicitly teaches providing a varistor with sputtering terminations whereas Ueda ostensibly teaches dipping. Thus, to combine the teachings of Ueda with Chan would change the principle of operation of Chan, thereby negating a finding of proper motivation to combine.

Further with respect to the rejection combining Ravindranathan in view of Ueda and further in view of the disclosed art in the present application, as argued previously Ravindranathan does not feature an untreated body surface. Although Ueda appears to teach an untreated body surface, it would not be obvious to combine Ueda with Ravindranathan since the latter reference requires the zinc phosphate layer 34 on the body 22 and to assert that it would have been obvious not to include this layer is untenable because it would render Ravindranathan

operating differently from the disclosed principle of operation. Accordingly, the Applicant respectfully submits that claim 39 is allowable over the prior art of record.

Dependent claims 40, 41, and 45-47, these are believed to be allowable at least by virtue of their dependency on independent claim 39.

With respect to claims 42-44, these claims are believed to be allowable at least by virtue of their dependency on independent claim 36.

With respect to independent claim 48, this claim is believed to be allowable for the reasons presented above with respect to independent claims 36 and 39.

Dependent claims 49-51, which depend from independent claim 48, are believed to be allowable at least by virtue of their dependency.

Claims 36-42, 44, 48 and 51 were further rejected under 35 U.S.C. §103(a) as being unpatentable over the disclosed art in the present application in view of Ueda. The Applicant respectfully traverses this rejection for the following reasons.

The discussed art in the present application, which includes U.S. Patent 5,115,221 to Cowman, U.S. Patent No. 4,316,171 to Miyabayashi et al. and U.S. Patent 5,614,074 issued to Ravindranathan, (which is the patent that issued from the parent application of Ravindranathan '263), as well as the text on pages 1 and 2 of the present application, do not teach or suggest a varistor featuring nickel barrier caps "formed by contacting the terminal regions but not the interior region of the semiconductor body with a nickel plating solution" where an interior region of body surface is not subjected to treatment or coding. Hence, the combination of Ueda with the disclosed prior art would not yield the features of the claims because, regardless of whether the nickel plating is deposited with sputtering, barrel plating or the putative dipping of Ueda, the disclosed conventional art still subjects an interior region of the body surface to treatment or coating.

Moreover, the Office Action asserts that forming barrier caps on an interior region is an admitted problem in that "leaching or creepage occurs when there is total immersion." It is unclear where this admission is found in the present application. Rather, the Office Action appears to mischaracterize and extrapolate the concept of solder leaching discussed in the background section of the present application to be the same concept as creepage of the plating material from end portions of a body. The problem of creepage due to total immersion is not a problem that is discussed in the present application. Thus, the asserted motivation given in present Office Action in making a rejection appears to be vacuous and without merit in light of the actual disclosed problems discussed in the present application. Nonetheless, in considering the asserted motivation on its face, proper motivation to combine these references is still lacking. As discussed previously, Ueda clearly illustrates extending electrode material a significant distance along the body of the thermistor element assembly 1 therein. Thus, the combination of Ueda with the disclosed prior art would not effect a varistor having nickel barrier caps formed by contacting terminal regions, but not an interior region of the semiconductor body, with a nickel plating solution without forming a nickel barrier over the interior region of the semiconductor body. Accordingly, the Applicant respectfully submits that claims 36, 42, 44, 48 and 51 are

patentable over the disclosed art in the present application in view of Ueda and requests that the rejection be withdrawn, accordingly.

In light of the foregoing comments, the Applicant respectfully submits that the claims are in condition for Allowance and request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BELL, BOYD & LLOYD LLC

BY

  
Patrick B. Law

Reg. No.41,549

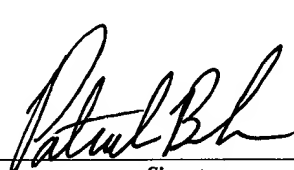
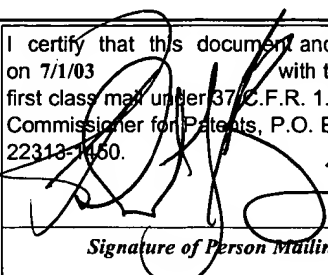
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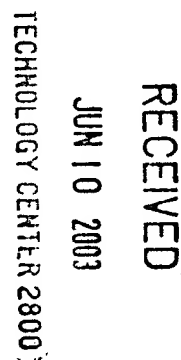
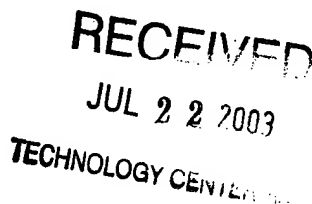
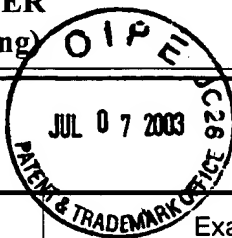
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Dated: July 1, 2003

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TRANSMITTAL LETTER (General - Patent Pending)			Docket No. 112690-895
In Re Application Of: Neil McLoughlin			
Serial No. 09/737,296	Filing Date December 18, 2000	Examiner K. Easthom	Group Art Unit 2832
Title: NICKEL BARRIER END TERMINATION AND METHOD			
<p style="text-align: center;"><u>TO THE COMMISSIONER FOR PATENTS:</u></p> <p>Transmitted herewith is:</p> <p><b>Request for Reconsideration on 4 pages and return receipt post card</b></p> <p>in the above identified application.</p> <p><input checked="" type="checkbox"/> No additional fee is required.</p> <p><input type="checkbox"/> A check in the amount of _____ is attached.</p> <p><input checked="" type="checkbox"/> The Director is hereby authorized to charge and credit Deposit Account No. 02-1818 as described below.</p> <p><input type="checkbox"/> Charge the amount of _____</p> <p><input type="checkbox"/> Credit any overpayment.</p> <p><input checked="" type="checkbox"/> Charge any additional fee required.</p> <p> Signature</p> <p>Dated: July 1, 2003</p> <p>Patrick B. Law (Reg. No. 41,549) Bell, Boyd &amp; Lloyd LLC P.O. Box 1135 Chicago, Illinois 60690 (312) 781-6801</p> <div><p>I certify that this document and fee is being deposited on 7/1/03 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.</p><p> Signature of Person Mailing Correspondence</p><p>Robert Buccieri Typed or Printed Name of Person Mailing Correspondence</p></div>			



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